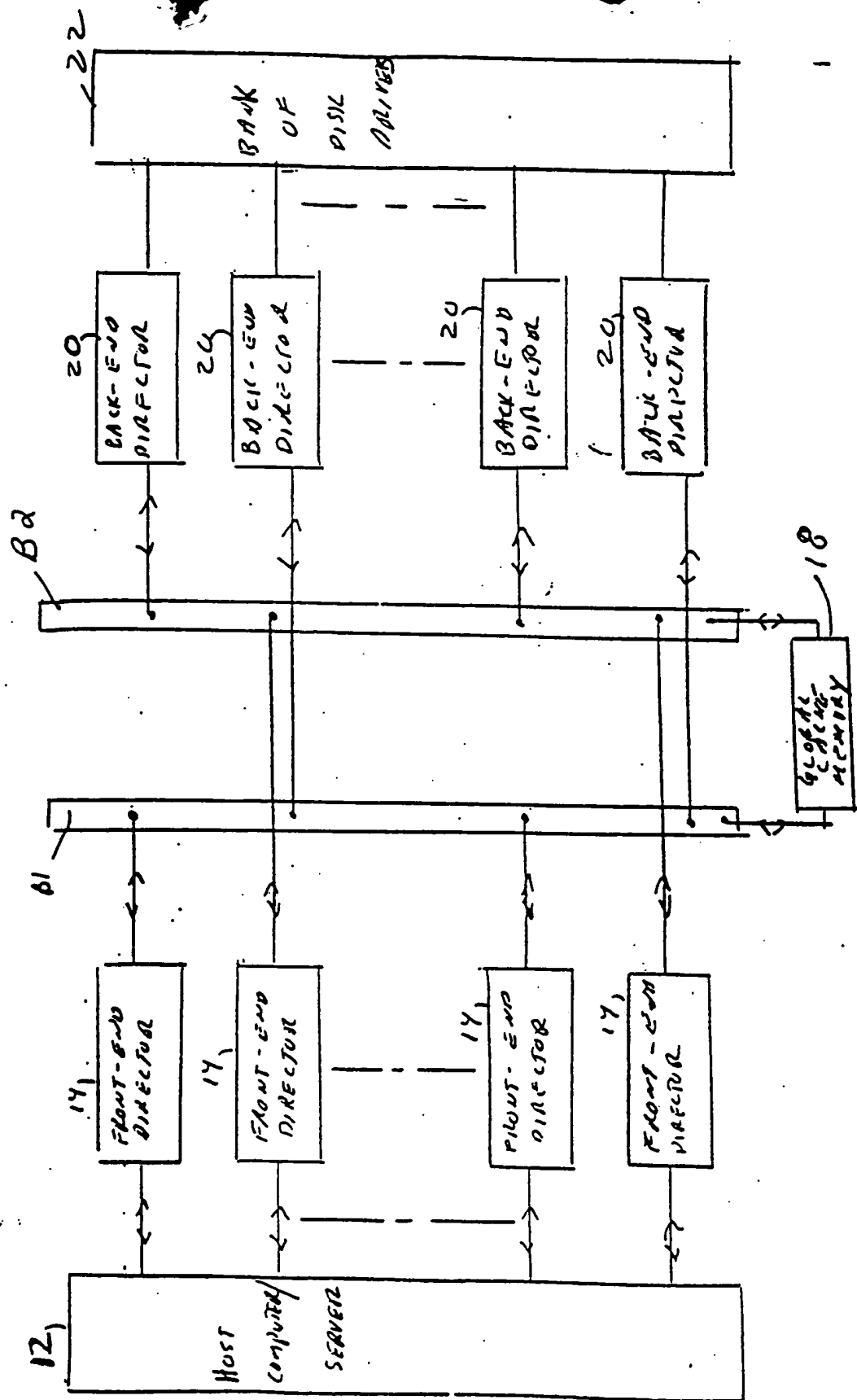


FIG. 1
SAN architecture



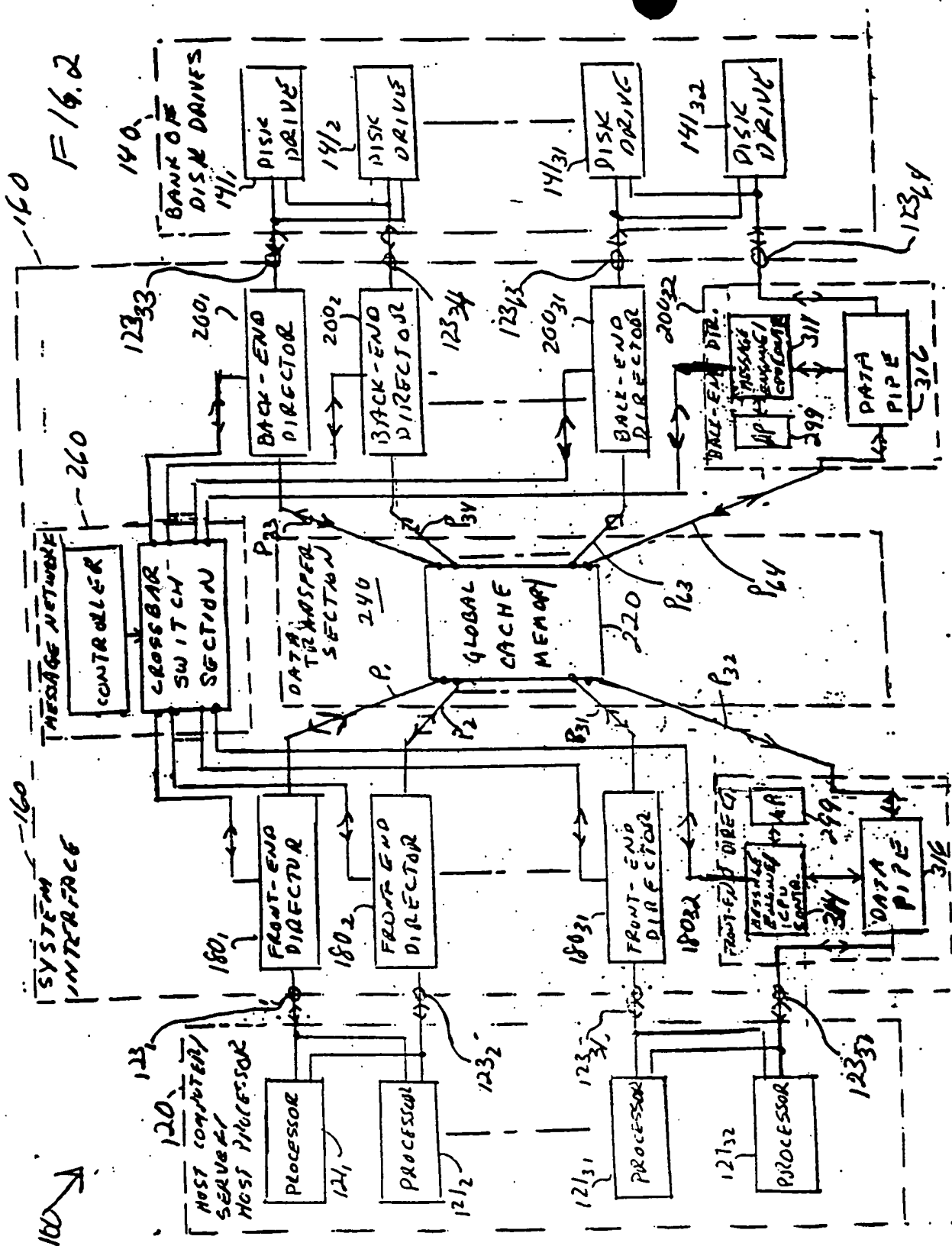


FIG. 3

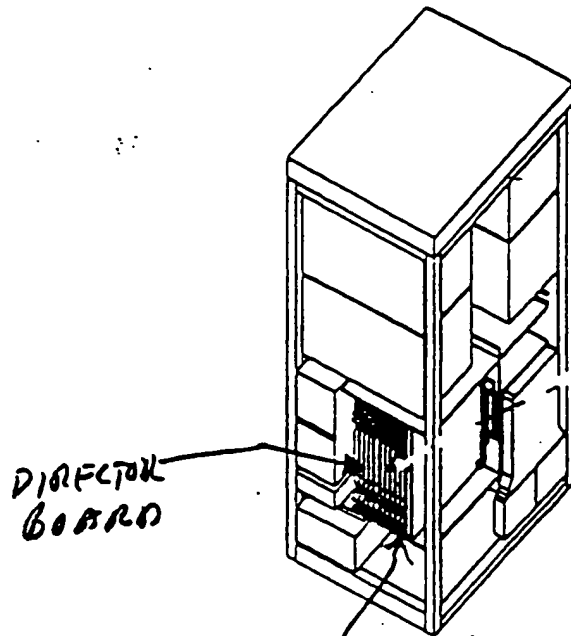
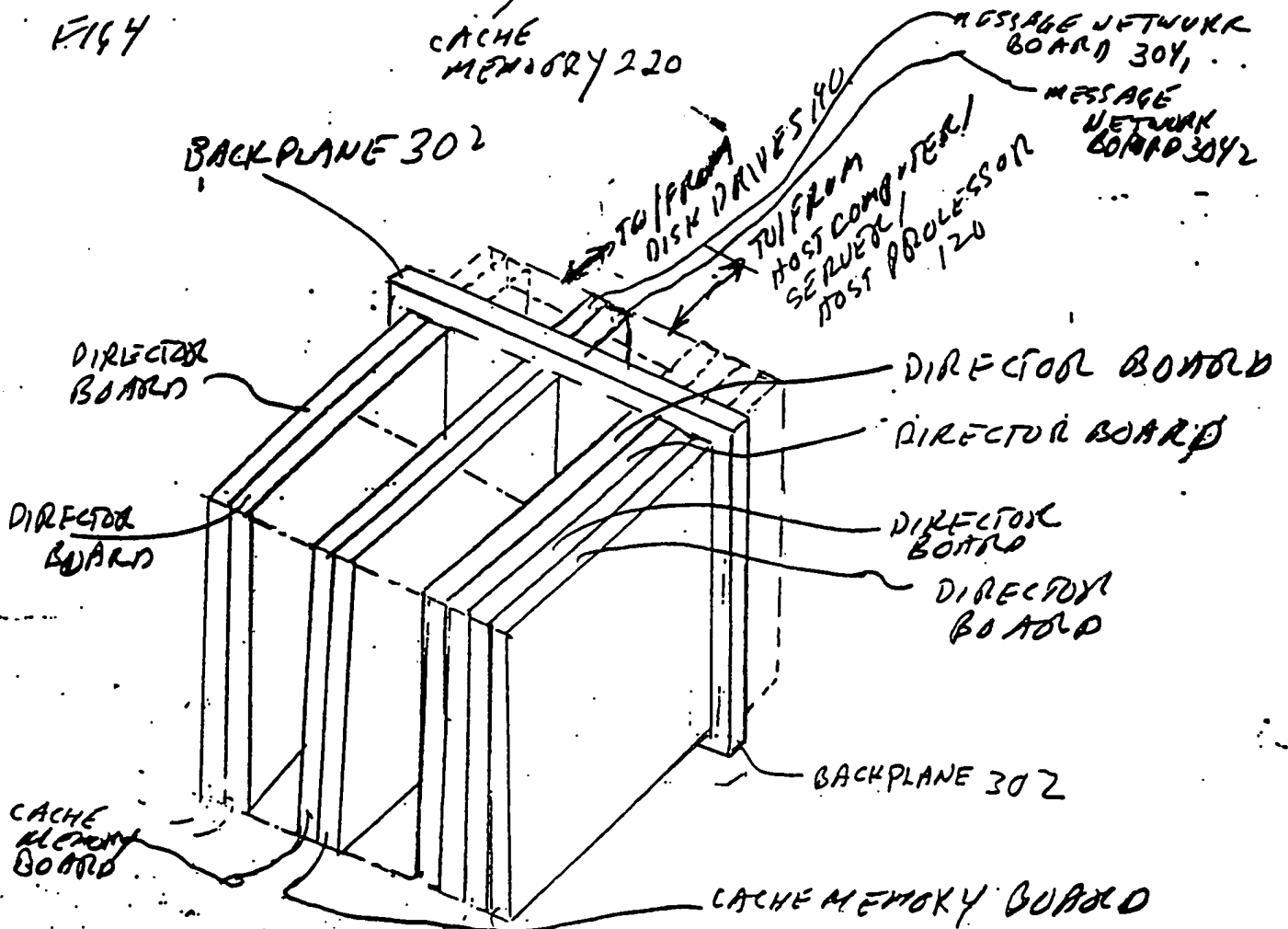
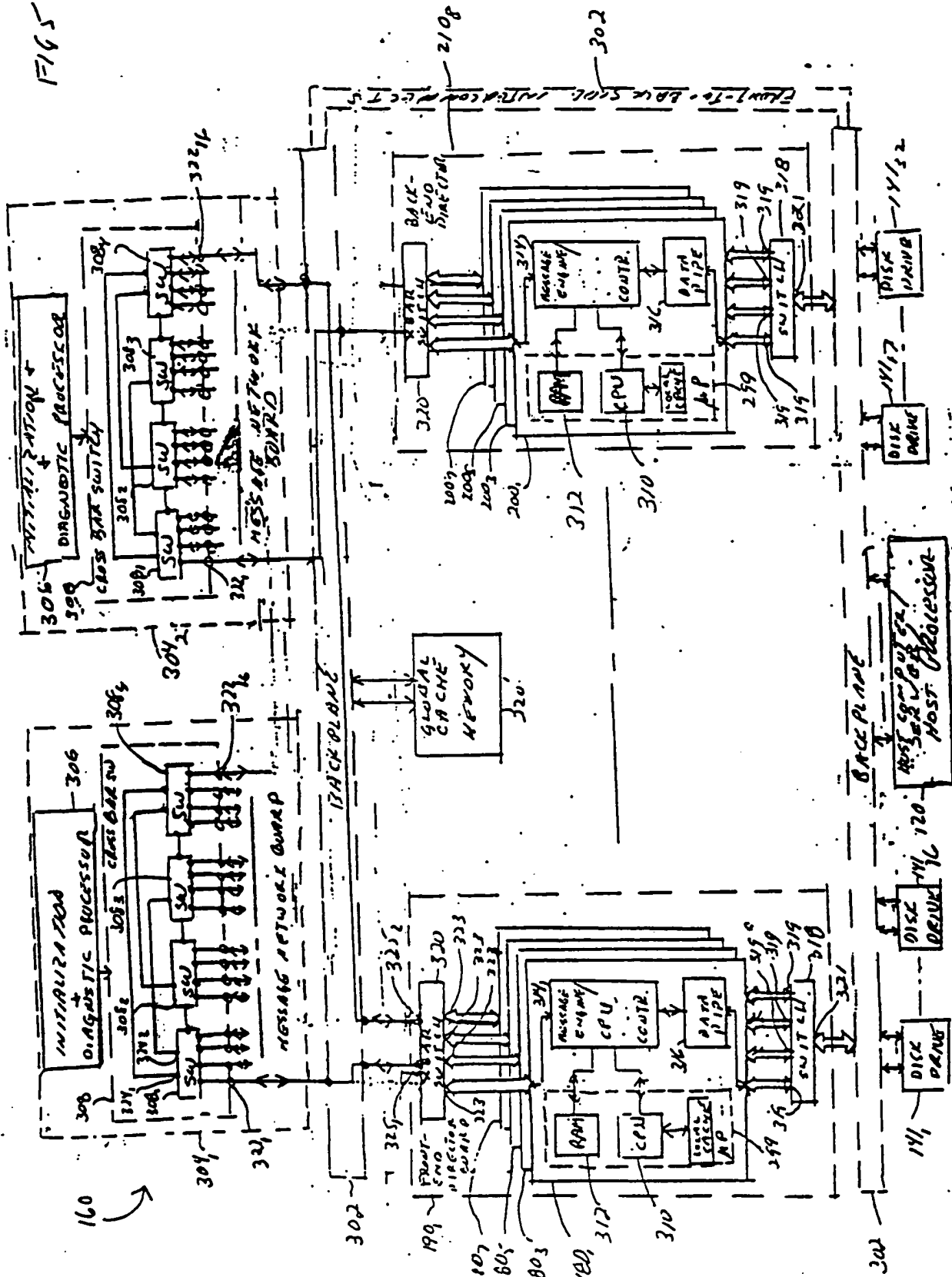
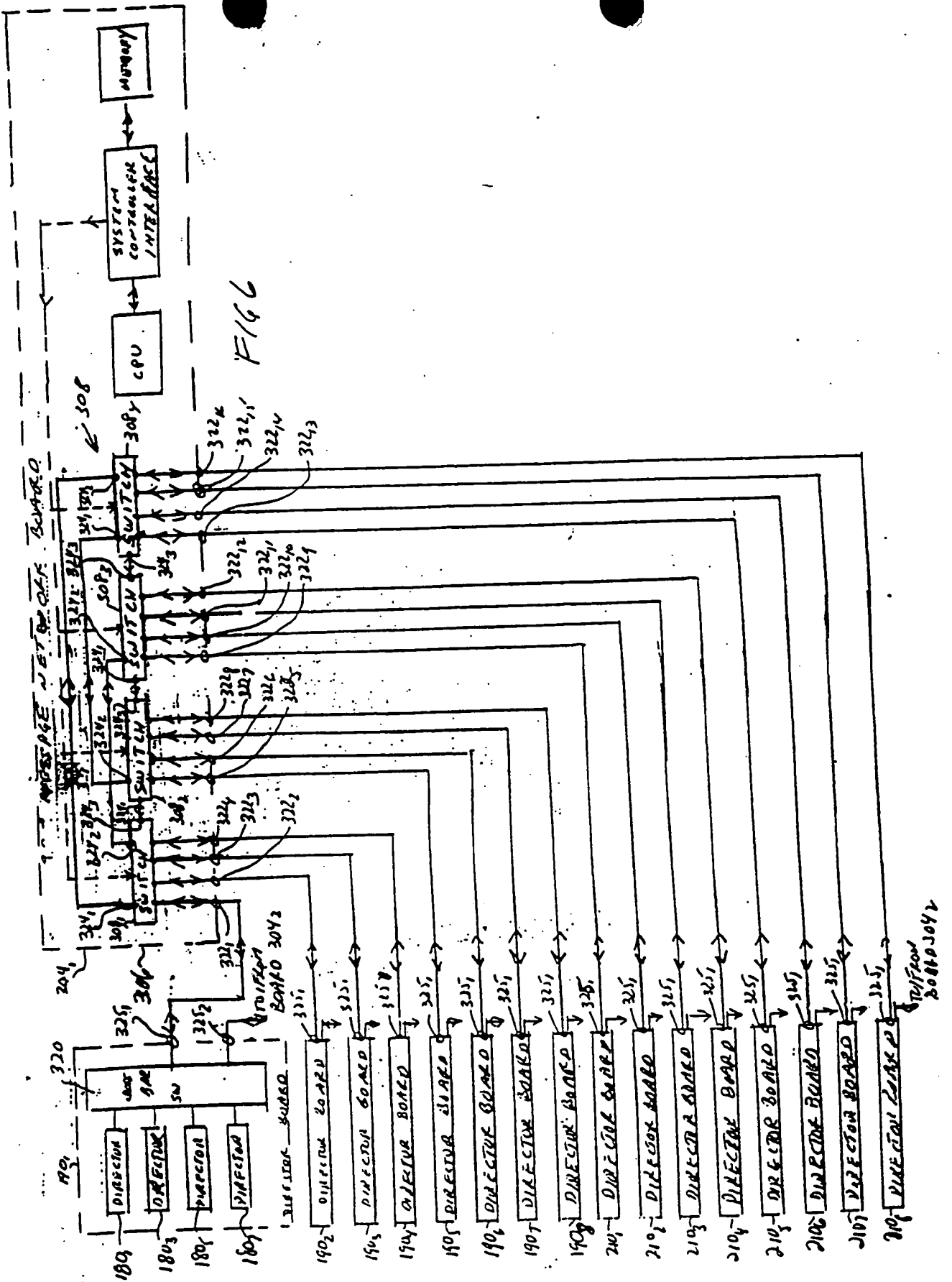


FIG. 4

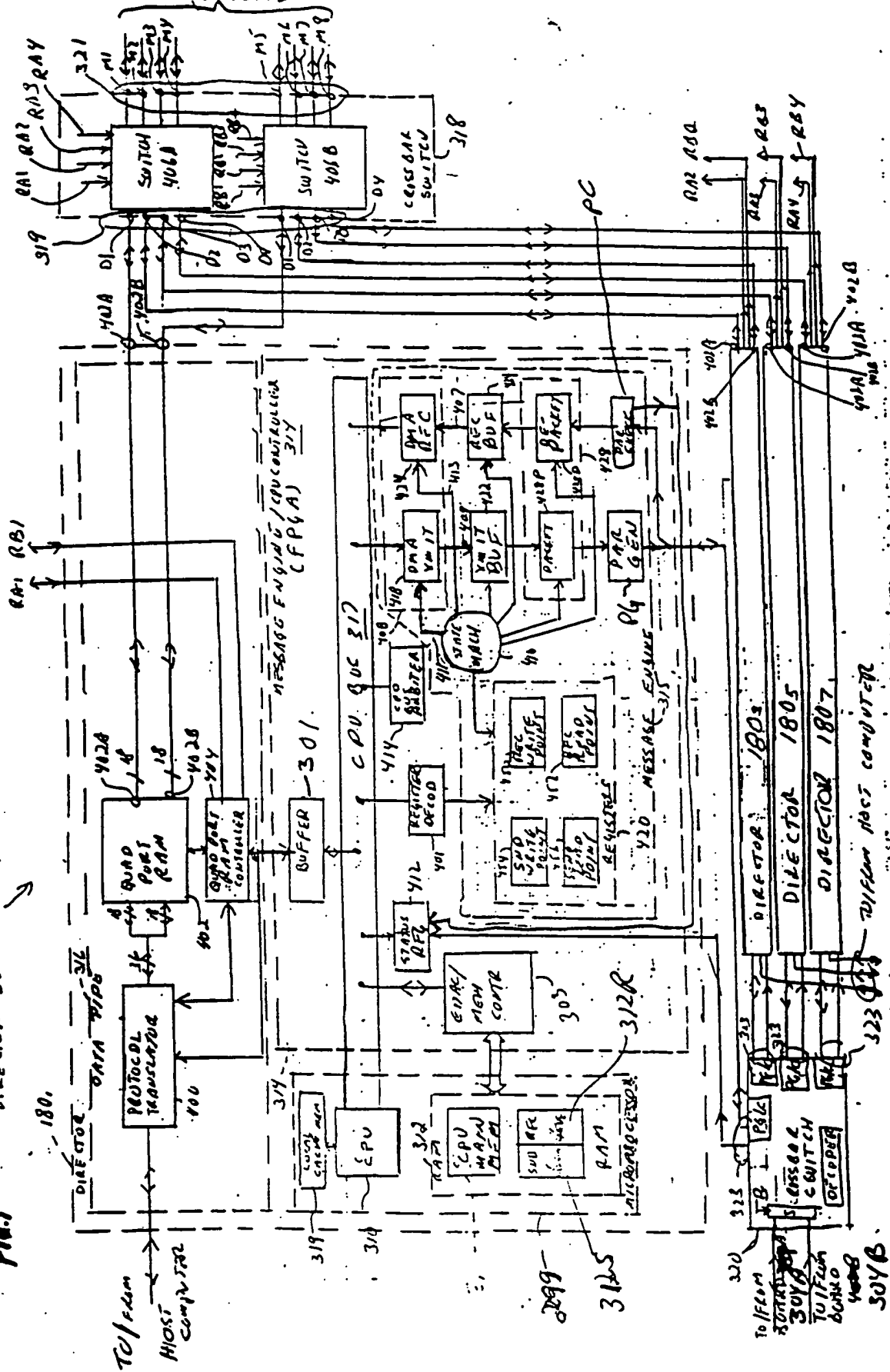


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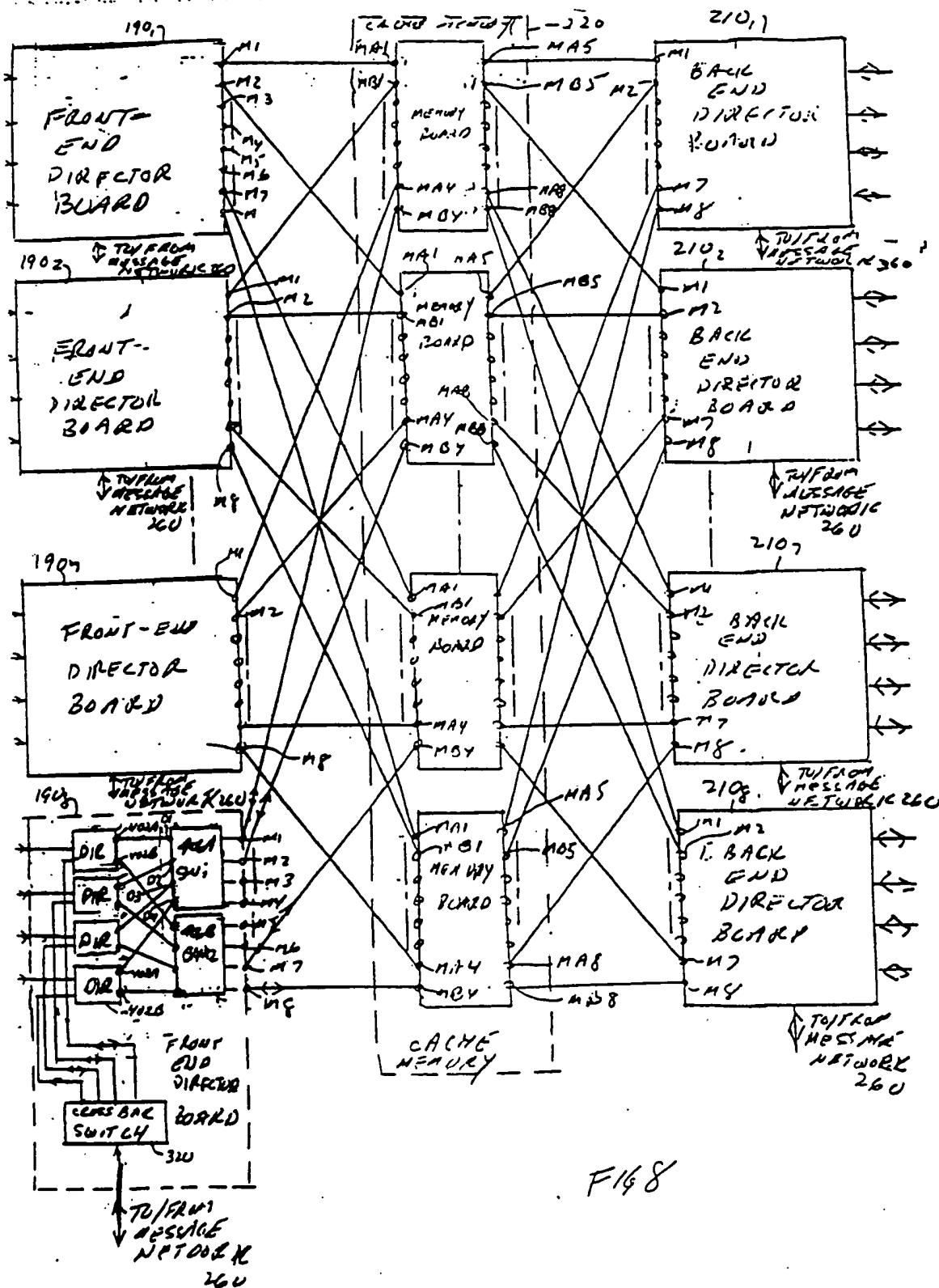


FIG 8

FIG 8A

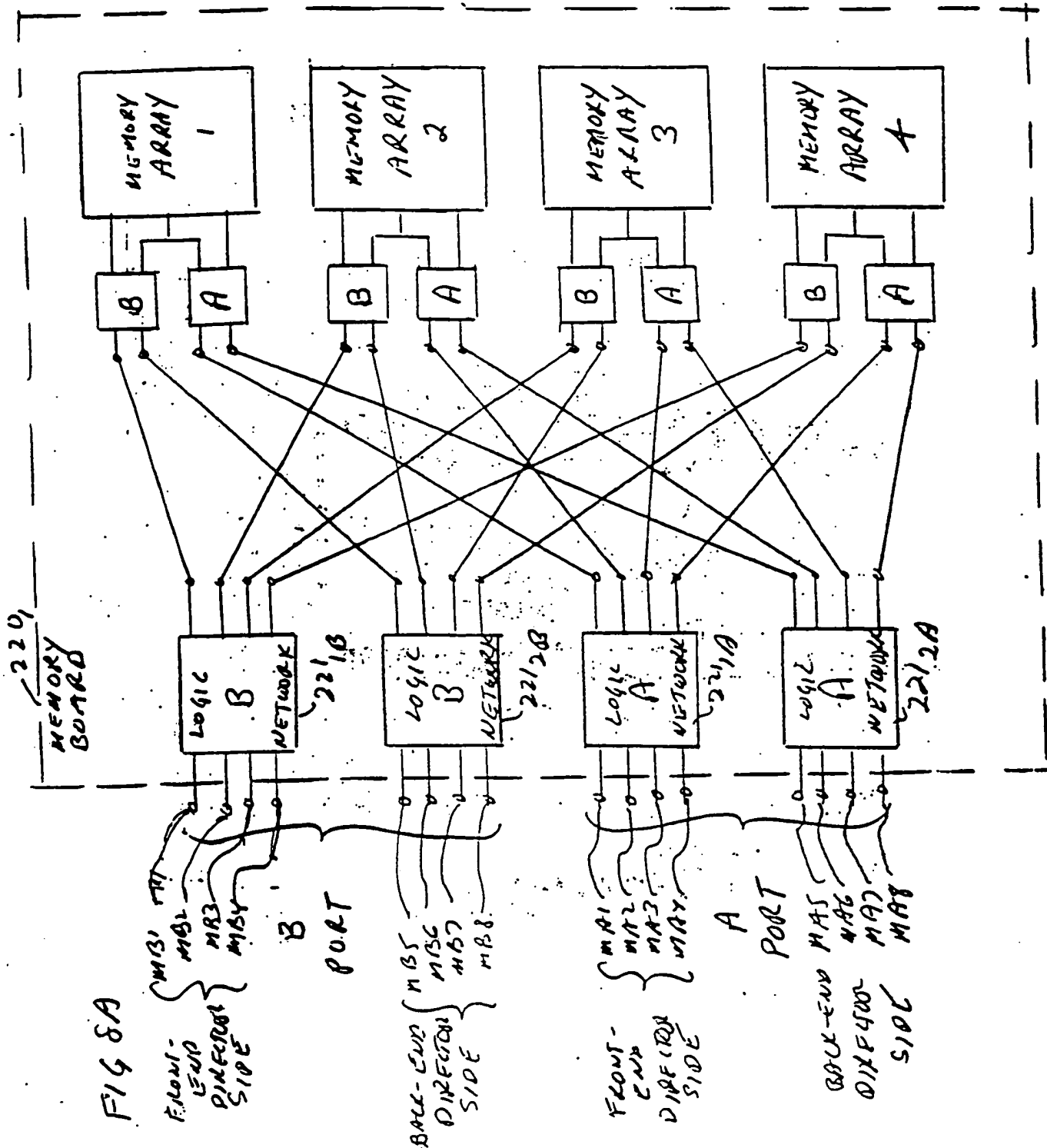
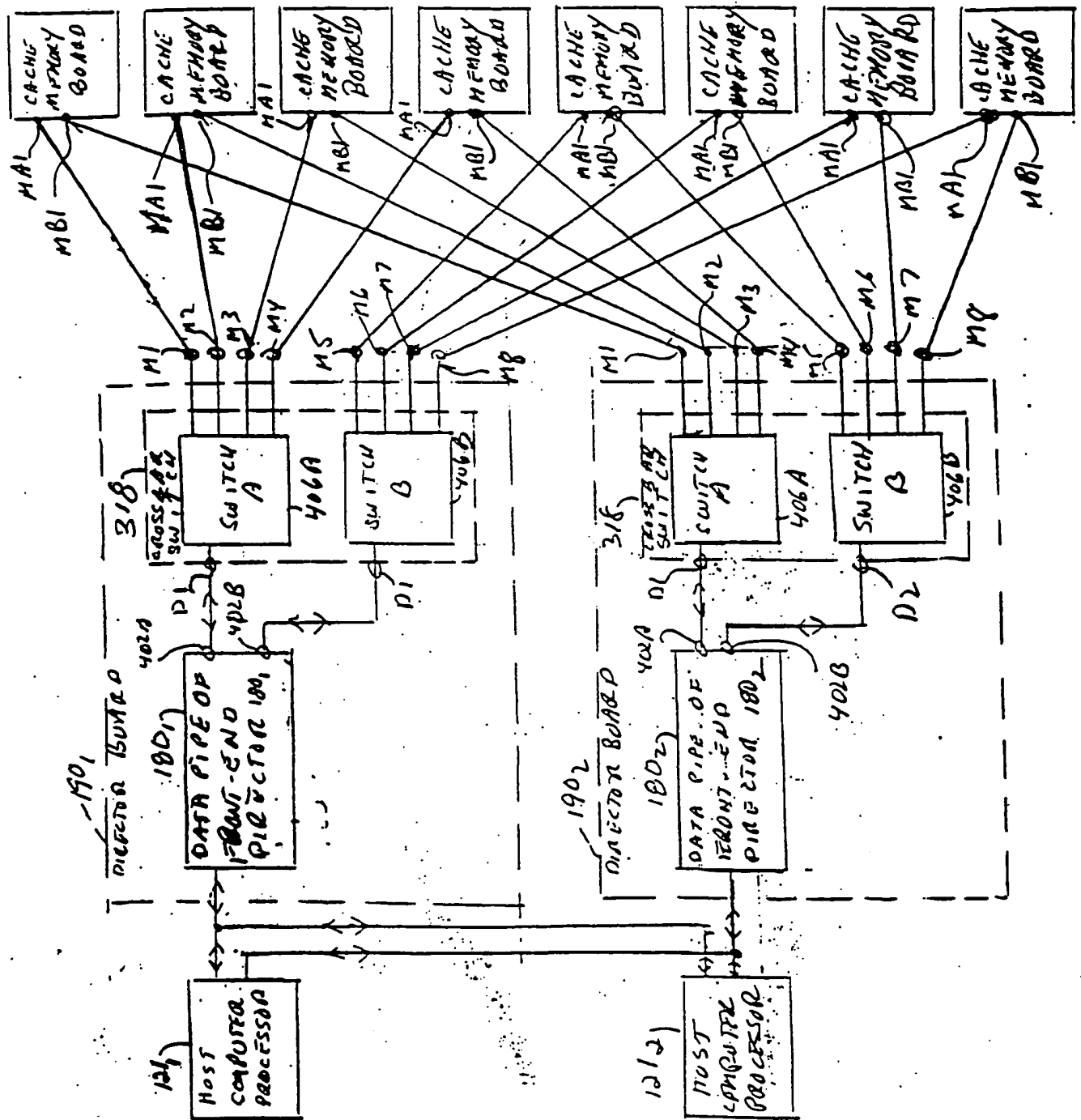


FIG 8B



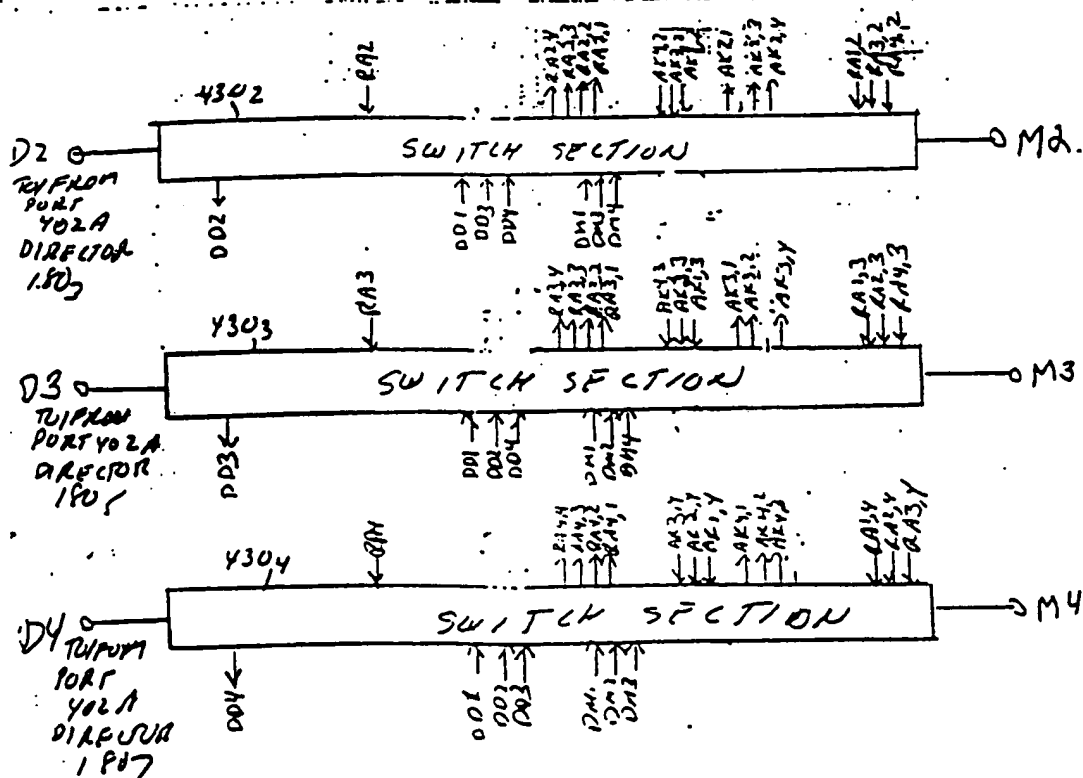
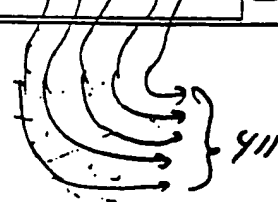
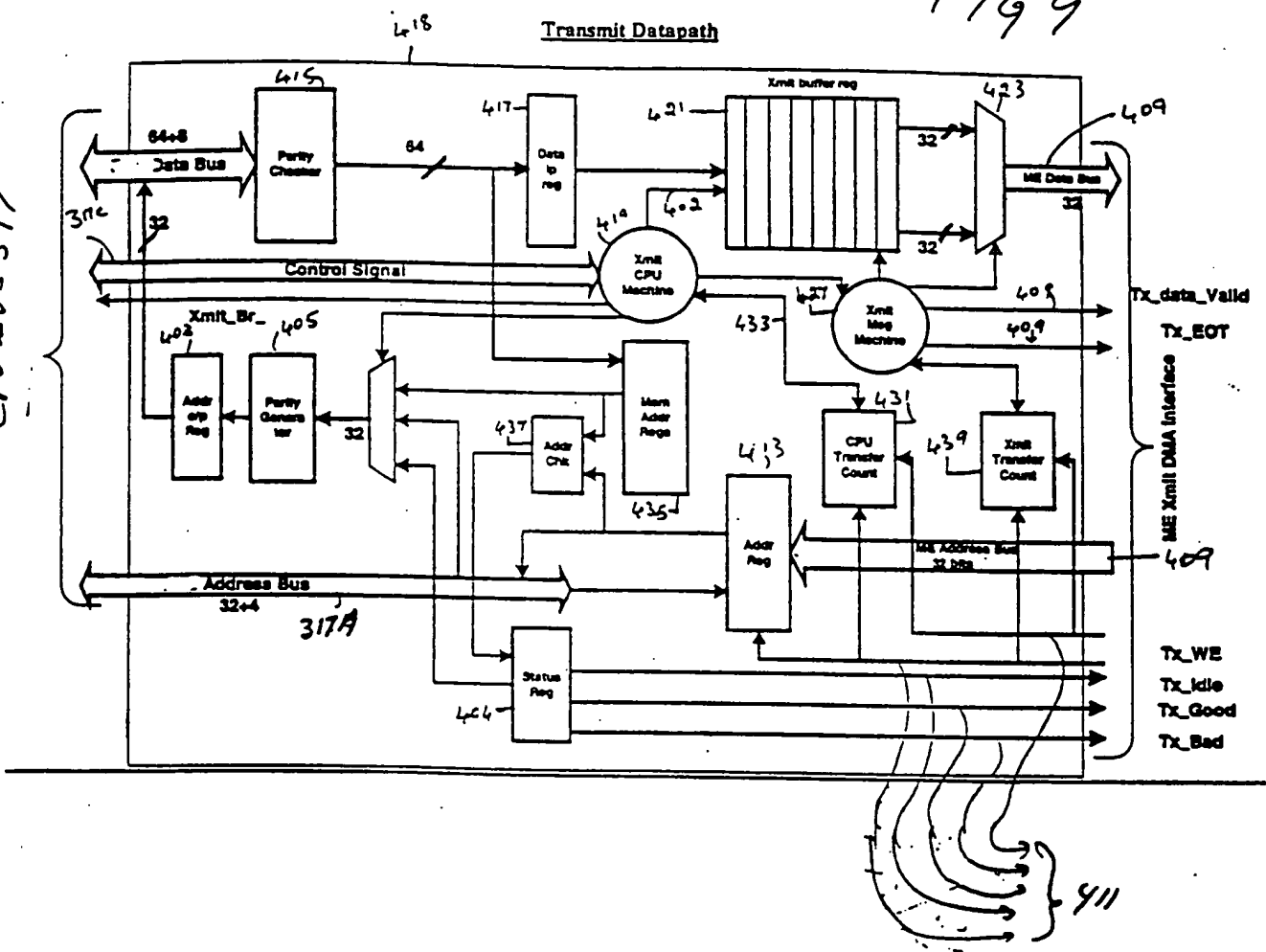


FIG 9

CPU BUS 317

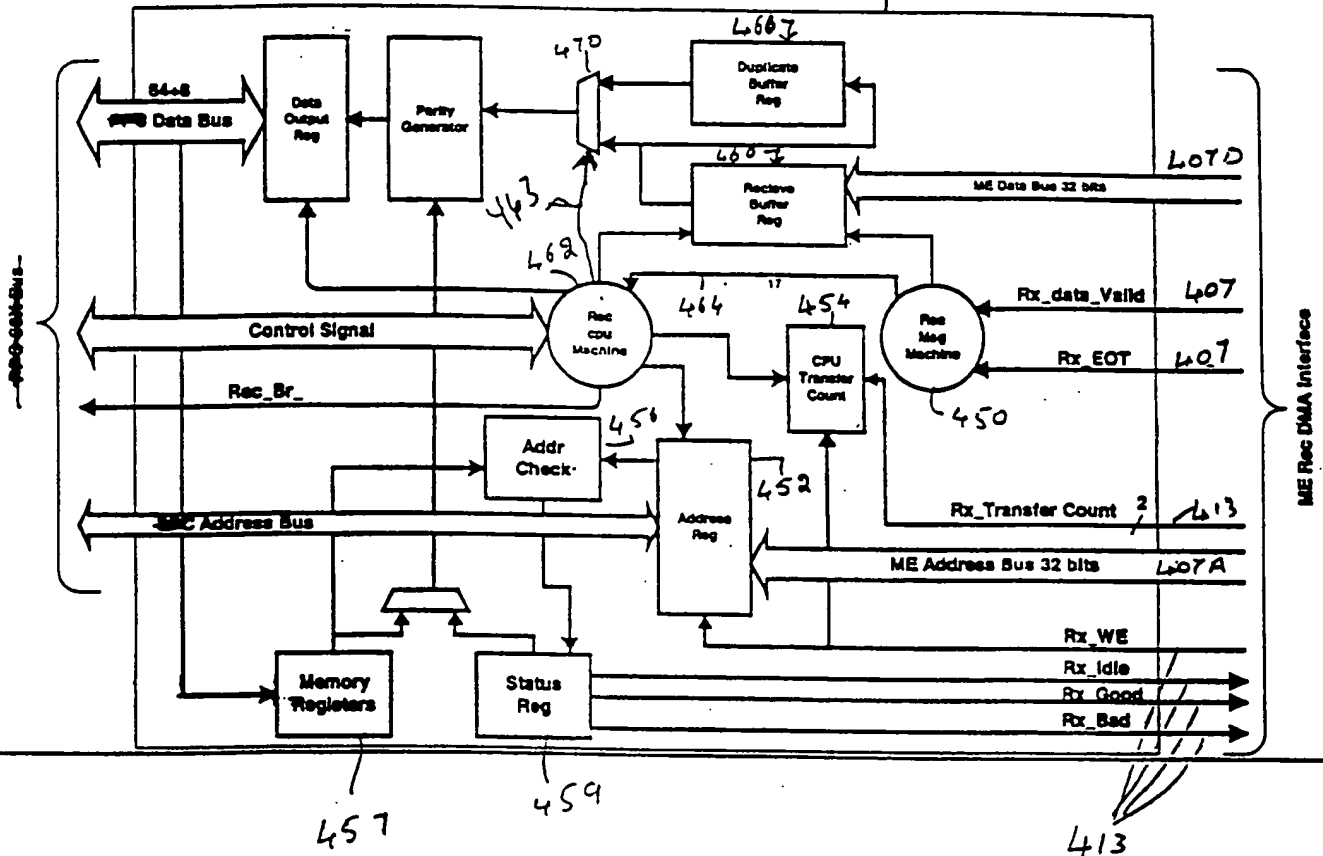


F1610

420

Receive Datapath

CPU BUS 317



Message Bus Send Operation

FIG. 11A

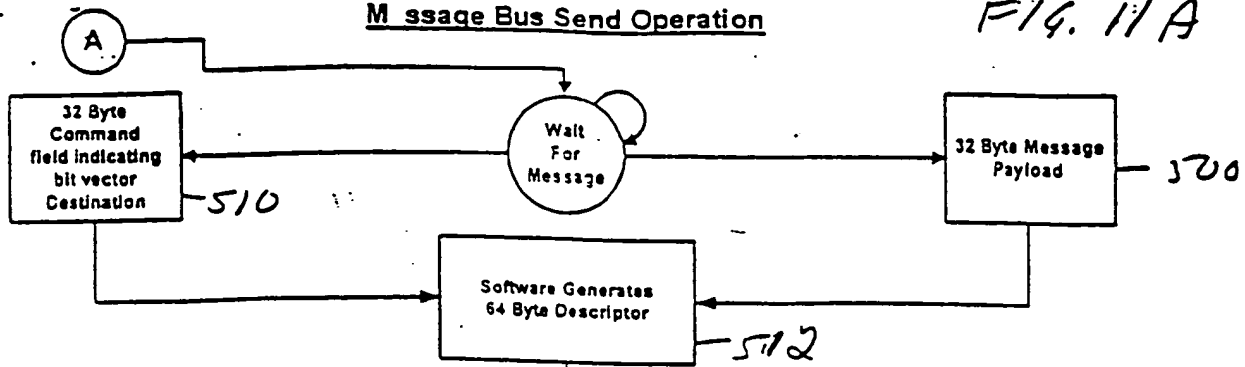


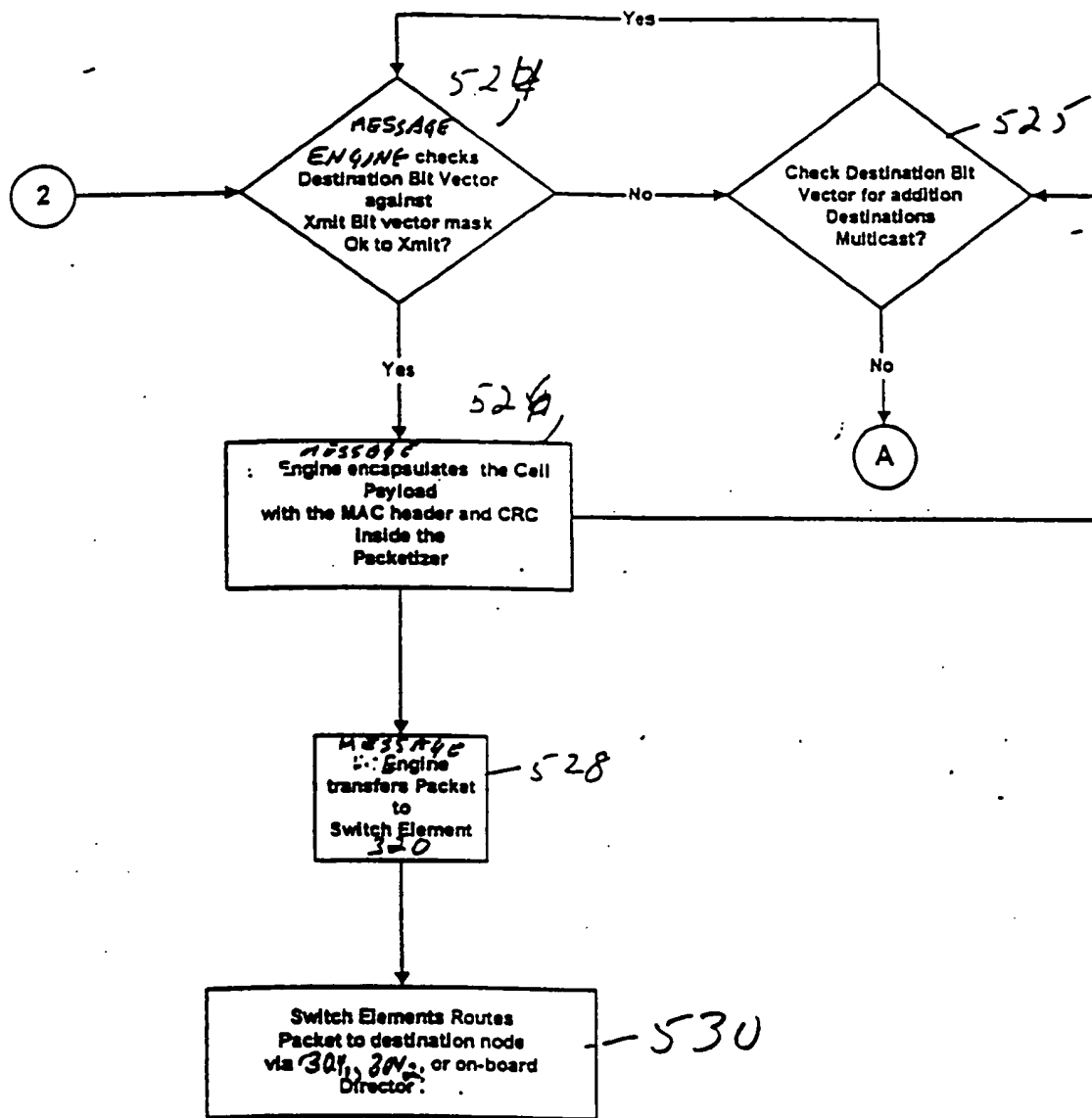
FIG. 11

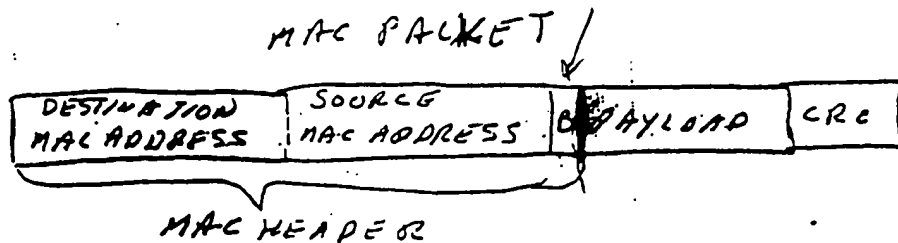
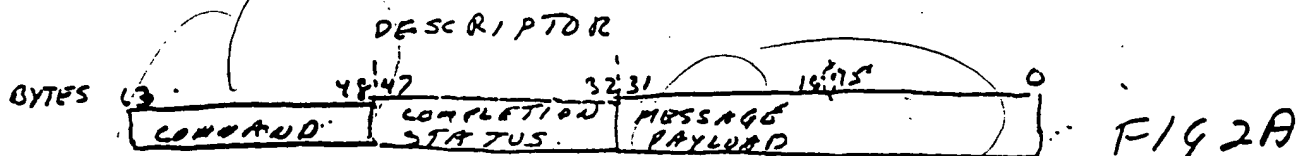
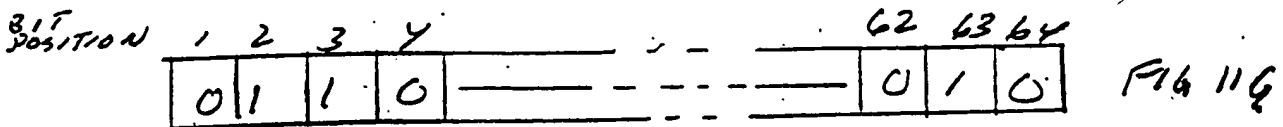
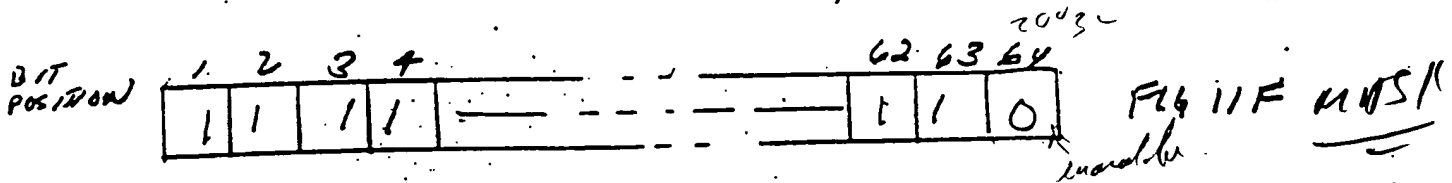
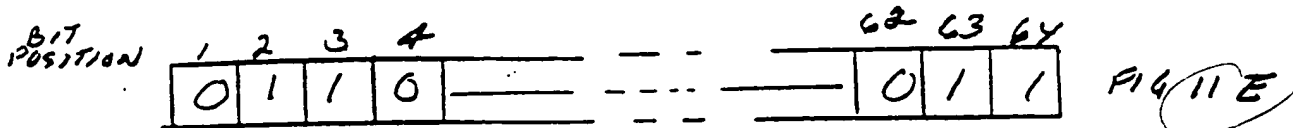
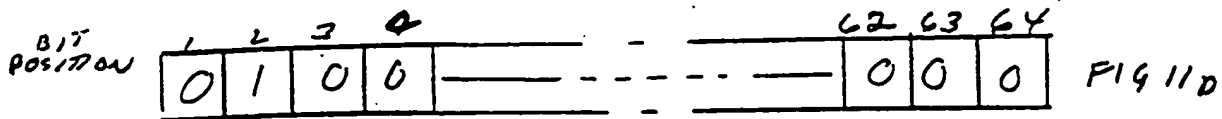
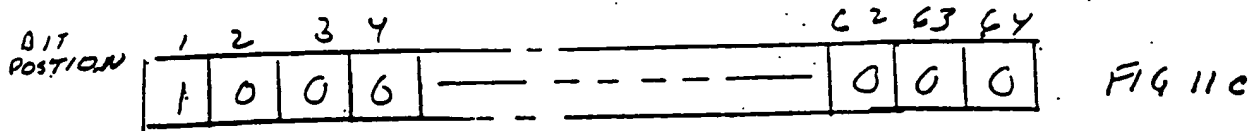
FIG. 11A

FIG. 11B

Message Bus Send Operation Continued

F1611B





Message Bus Receive Operation

FIG. 12A

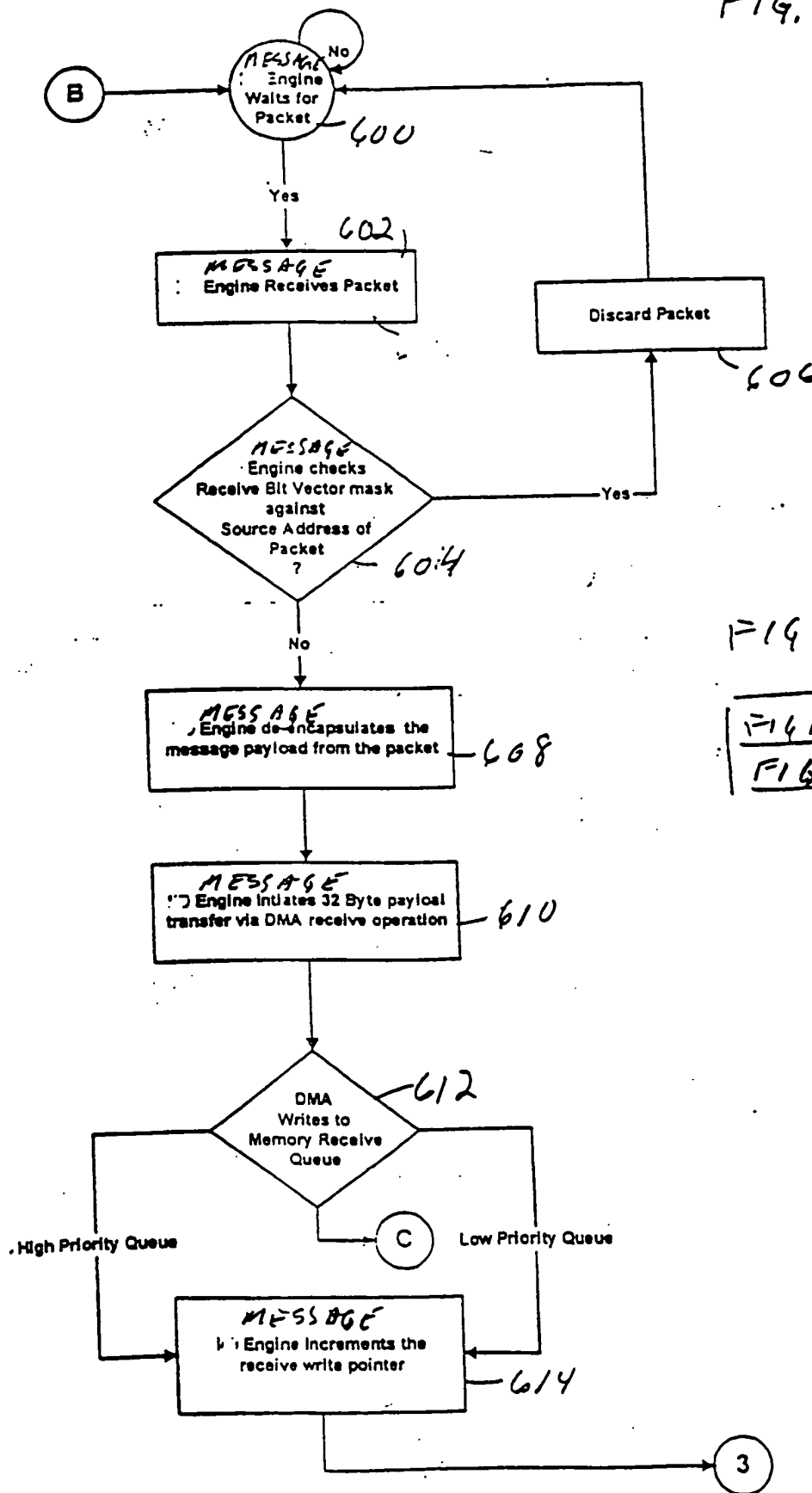
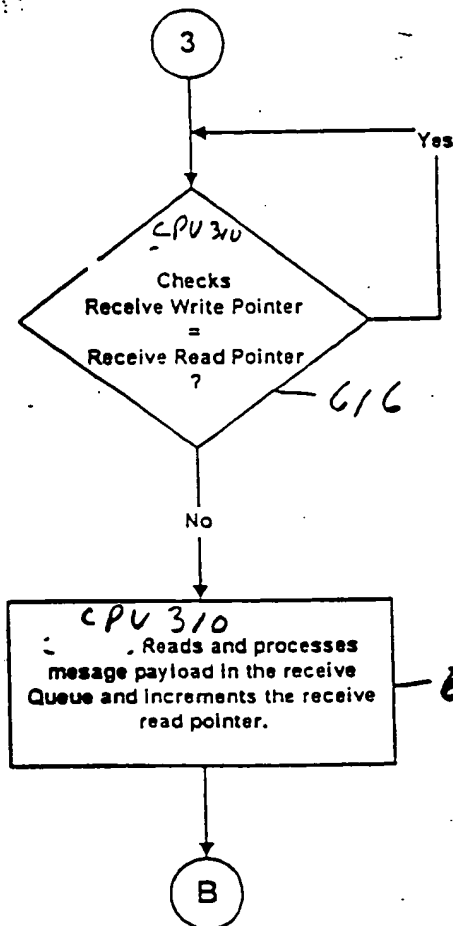


FIG. 12

FIG. 12A
FIG. 12B

Message Bus Receive Operation Continued



F-1412B

Message Bus Acknowledgment Operation

F14.13

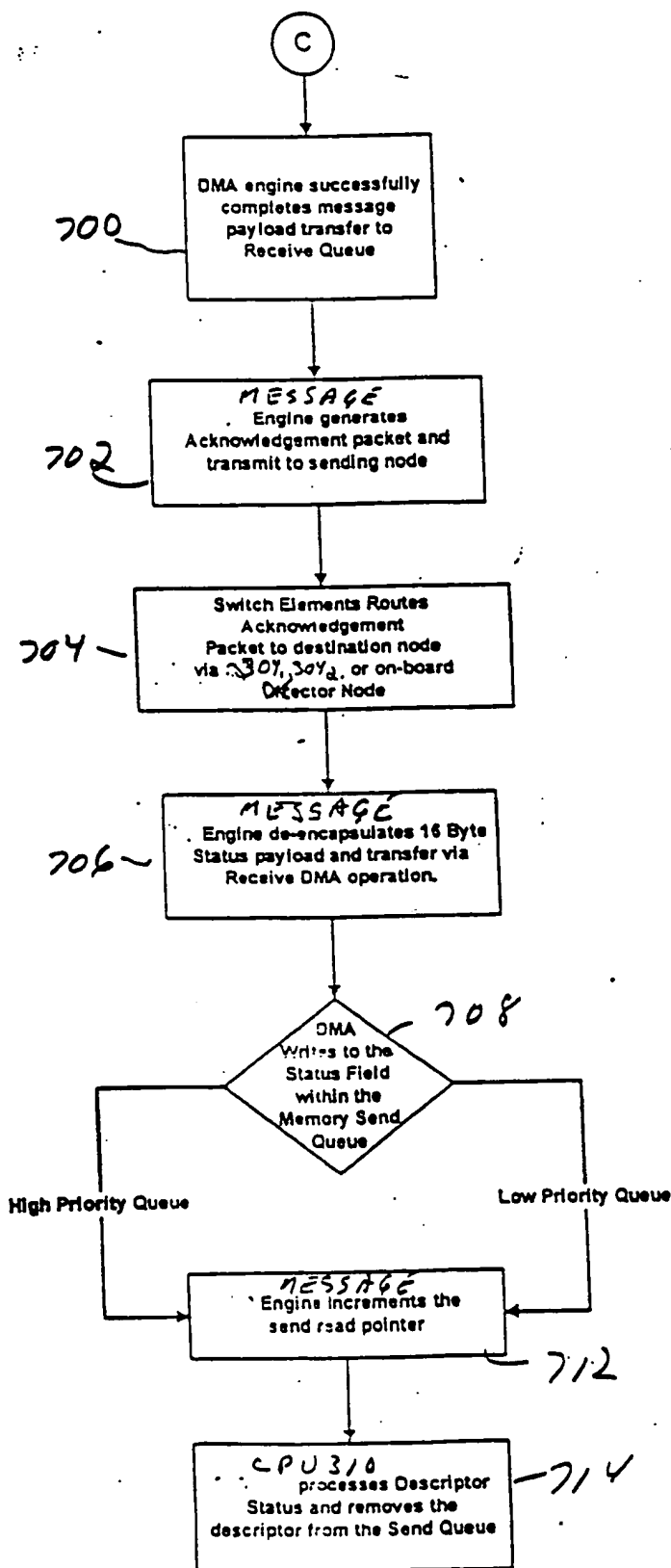
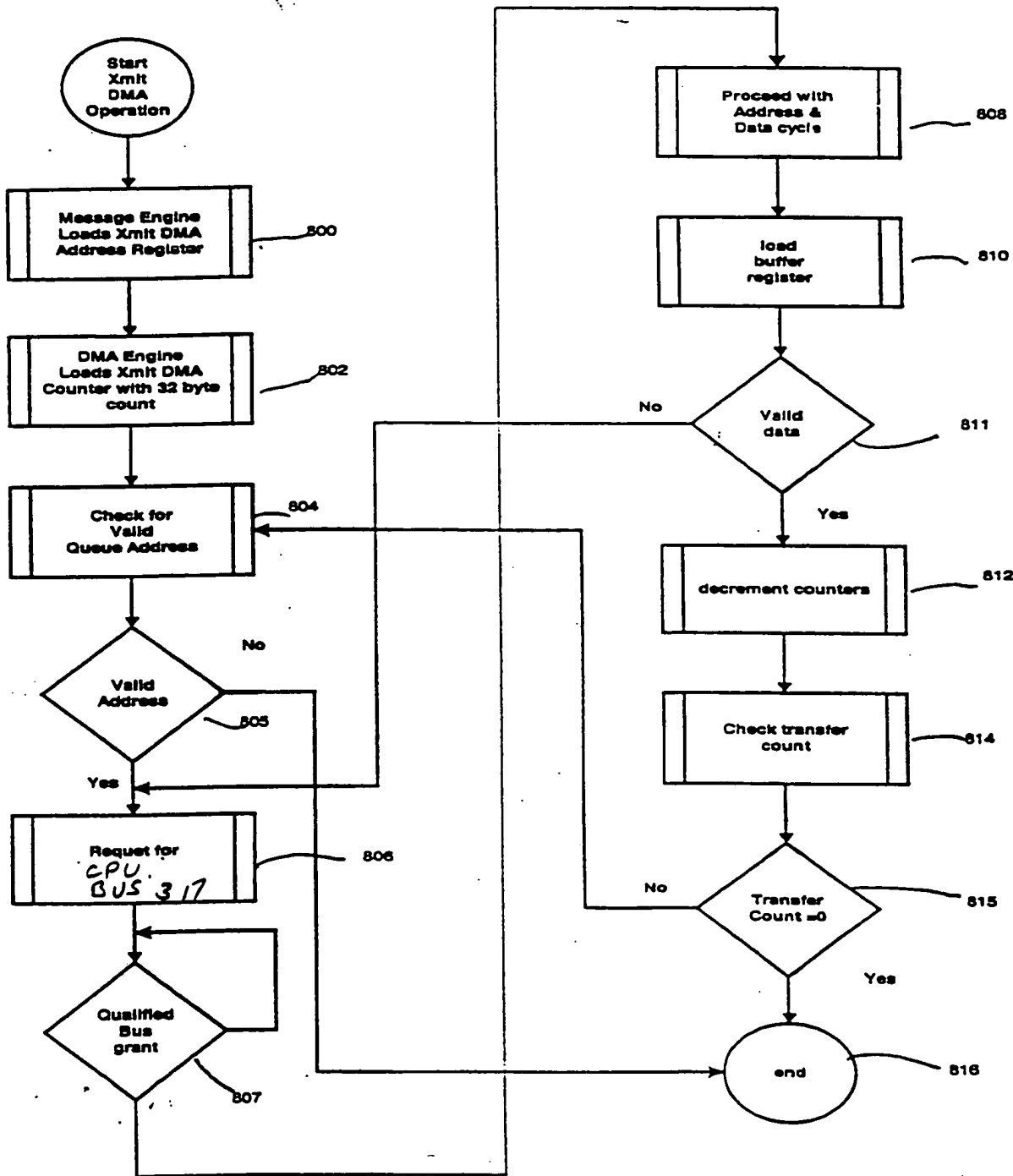


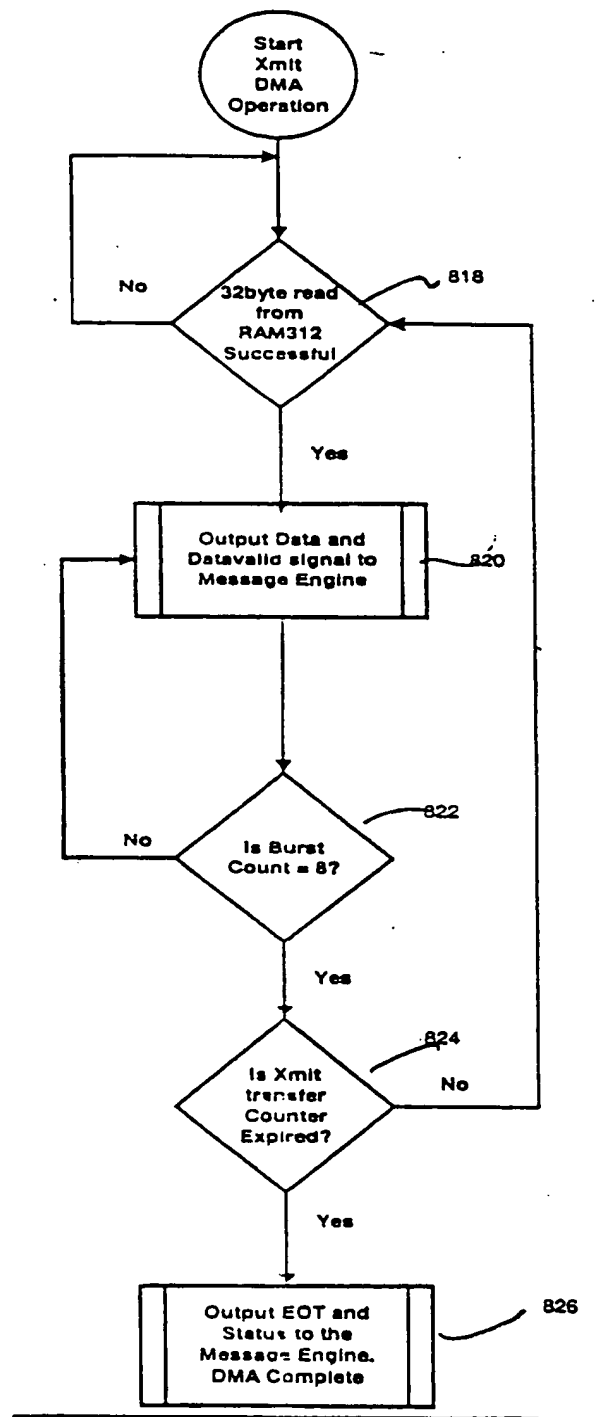
FIG 1AA

Xmit CPU flow



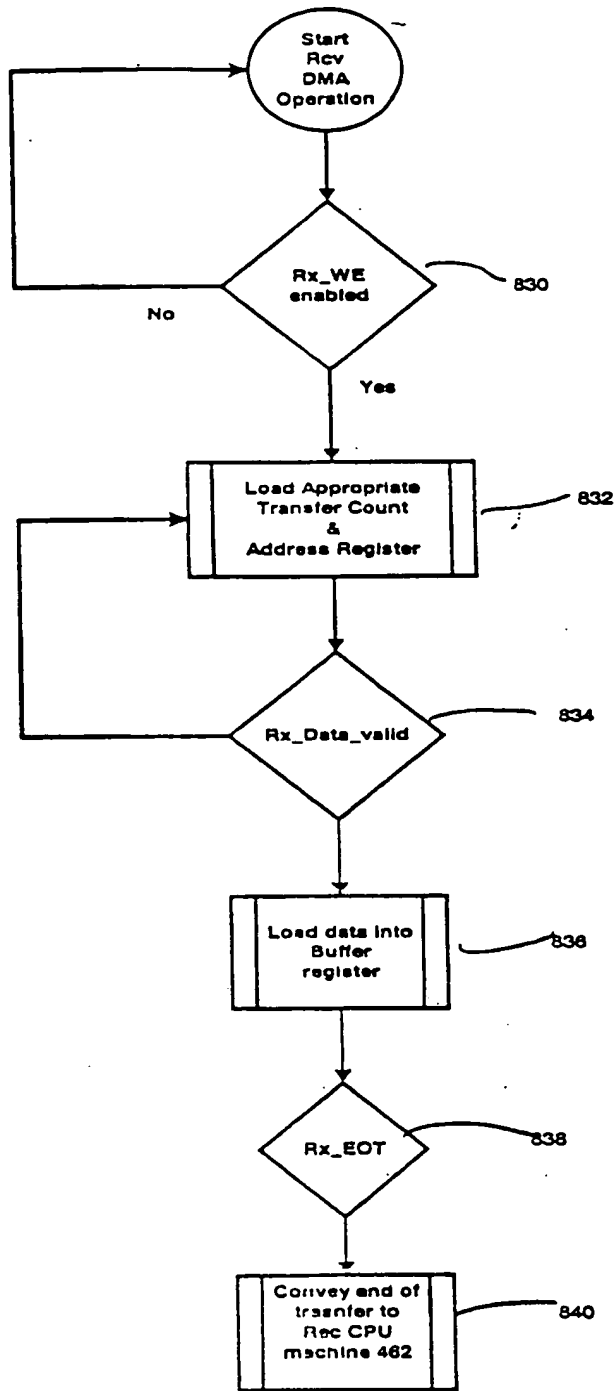
F1414B

Xmit Msg fl w



F1615A

Rec msg fl w



F1615B

Rec cpu flow

